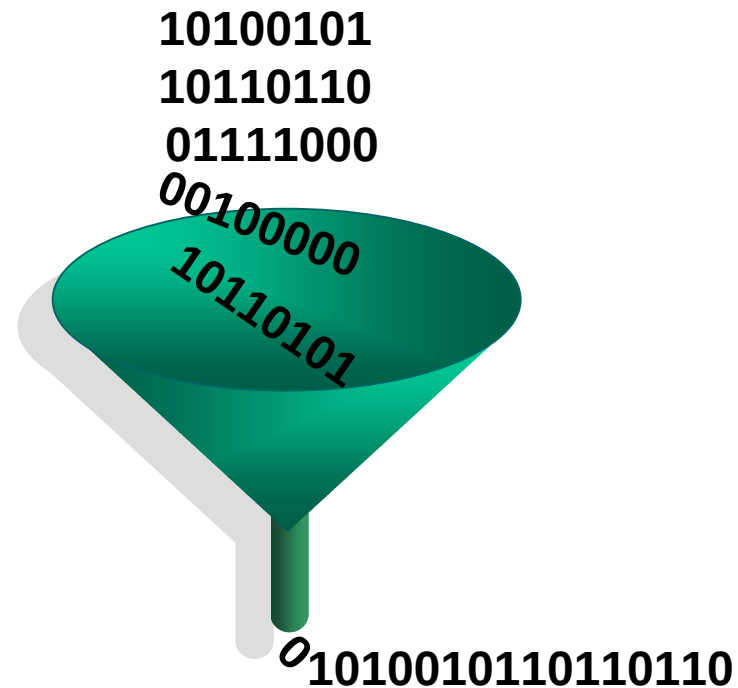


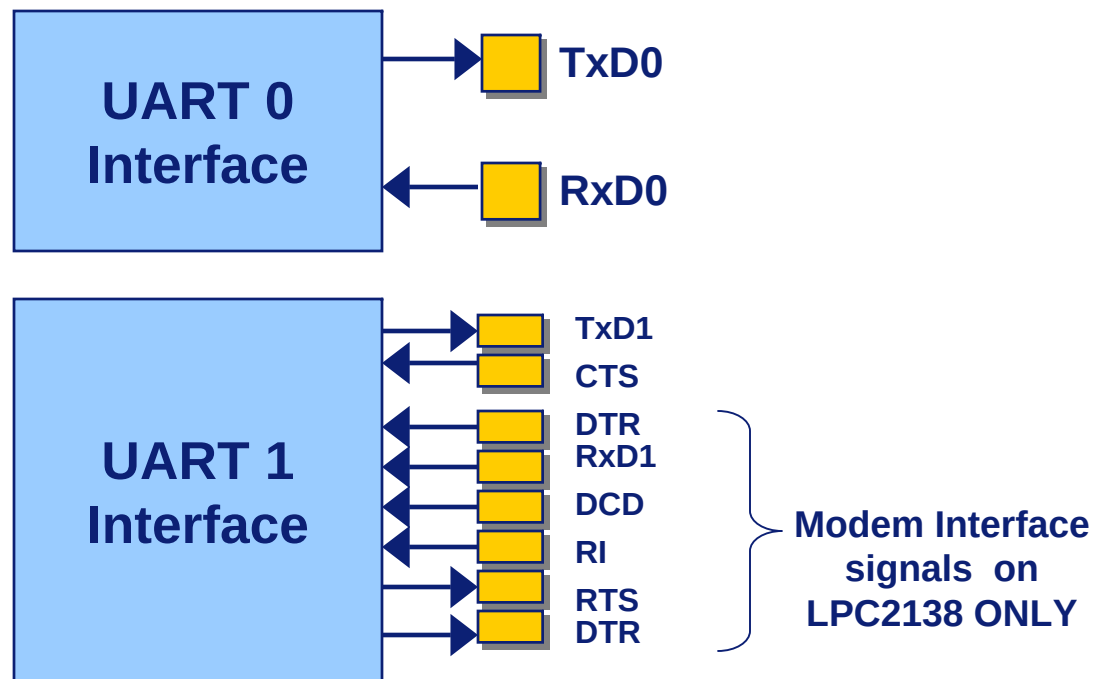
Serial Communication Interfaces

Serial Communication Interfaces

- UART0 / 1
- 2 I²C Interfaces
- SPI Interface
- SSP Interface



UART0 / UART1



Maximum possible speed of the UART
3.75 Mbits/sec

UART0 / UART1

- Register locations conform to '550' industry standard UART
- Built-in Baud Rate Generator
 - 16-bit baud rate generator clock divisor made from 2 8-bit divisor registers: DLM (MSB), DLL (LSB)
 - Required baud rate: $pclk/(16 * Divisor)$
- Error Detection
 - Parity, Framing and Overrun Errors detected
 - Break Interrupt detection

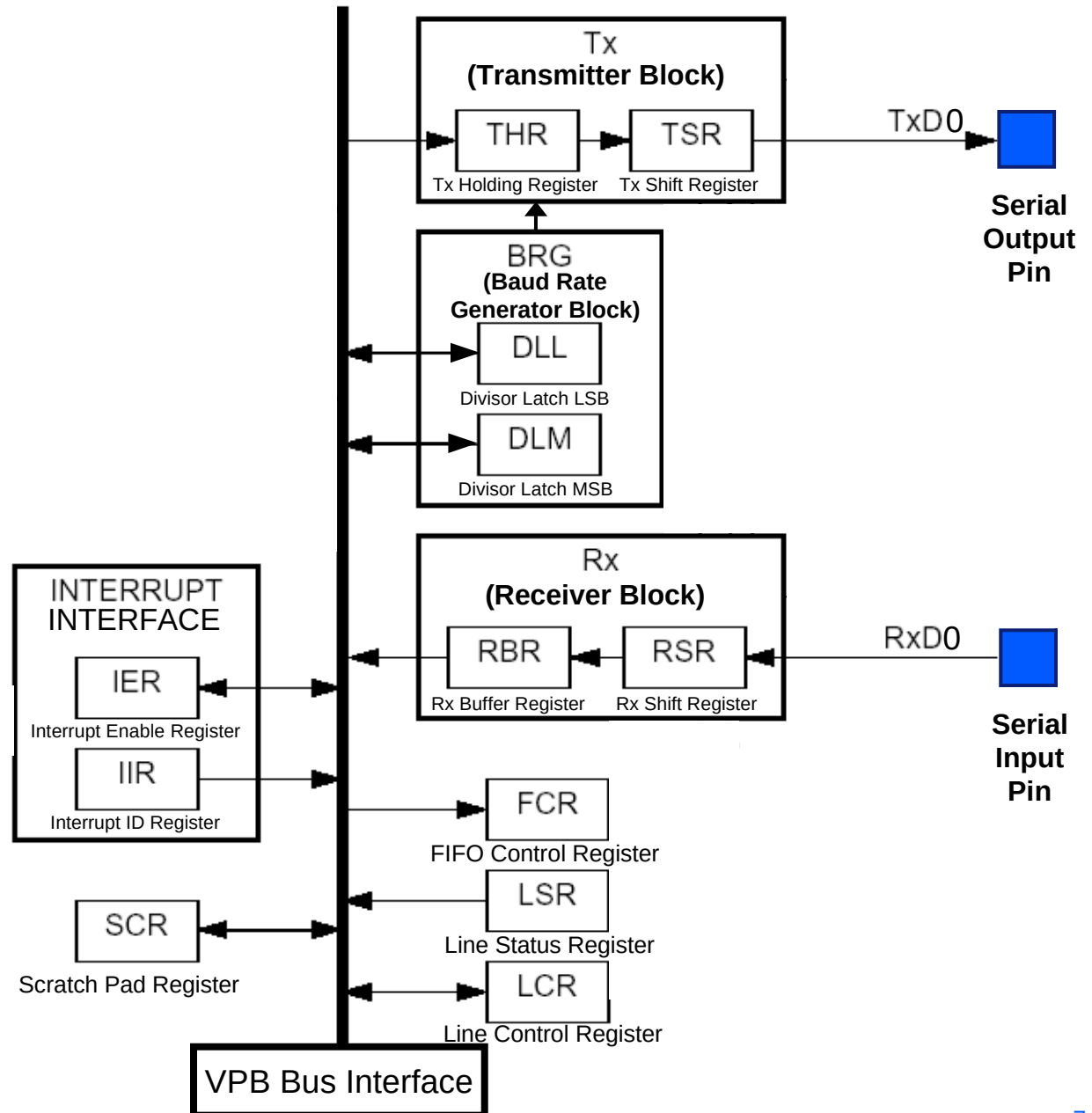
UART0 / UART1 (cont.)

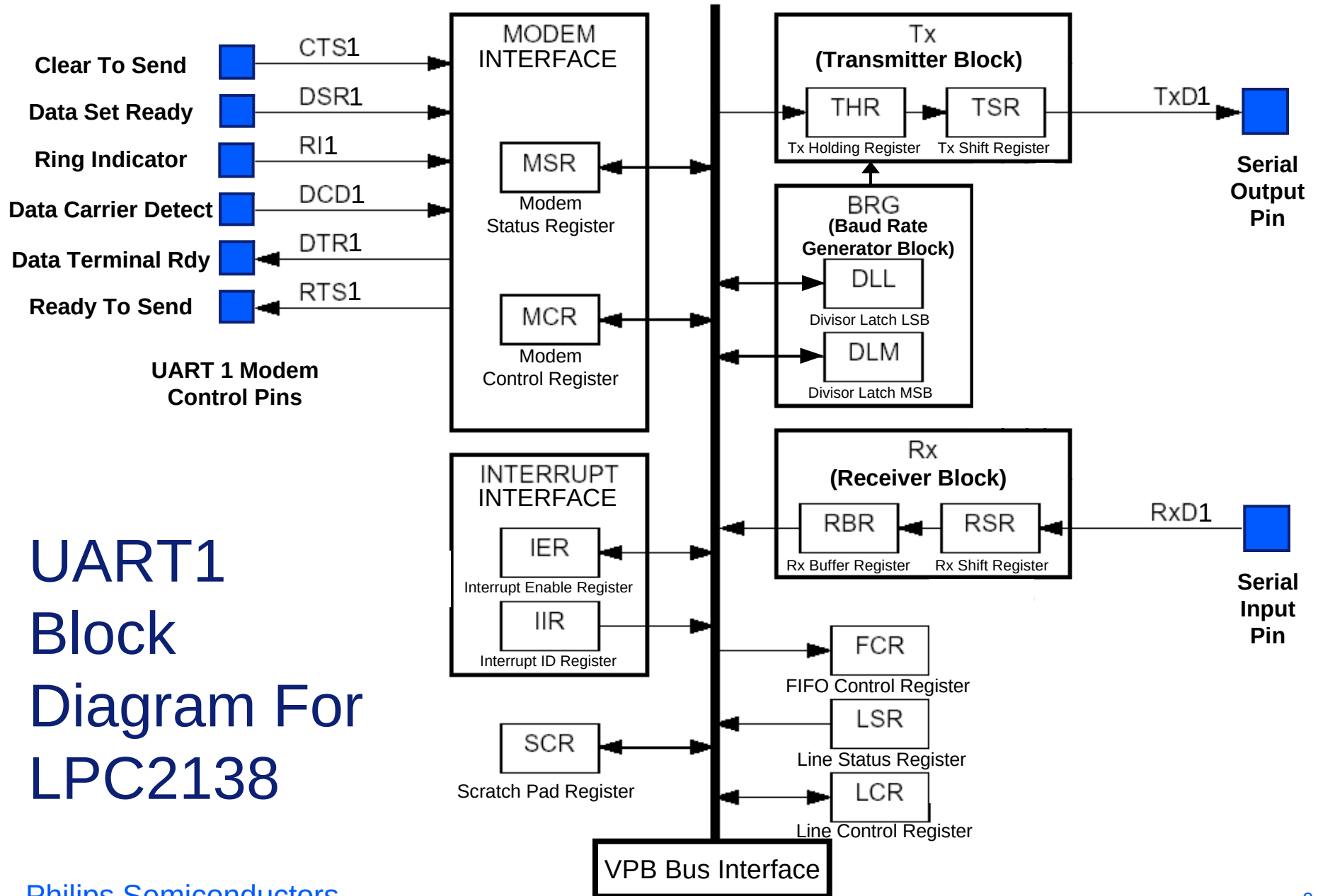
- 16 byte Receive and Transmit FIFOs
 - Receive FIFO trigger points at 1, 4, 8, and 14 bytes
 - Break signal can be transmitted
- Word Length Select: 5, 6, 7 or 8-bit characters
- Stop Bit Select: 1 or 2 stop bits
- Parity Select: Odd or Even parity

UART1 on LPC2138

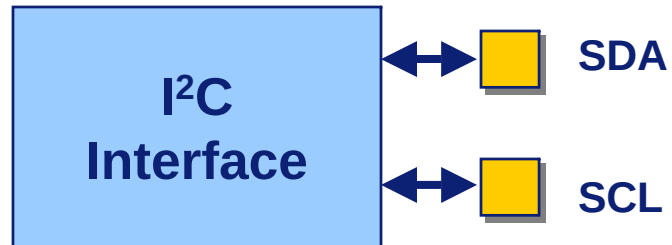
- Standard modem interface signals included (UART1)
- Transmit bit added (in Transmit Enable Register) so that transmission can be immediately halted if flow control signal is deactivated

UART0/1 Block Diagram





I²C Bus Interface



Maximum possible speed of the I2C
400Kbits/sec

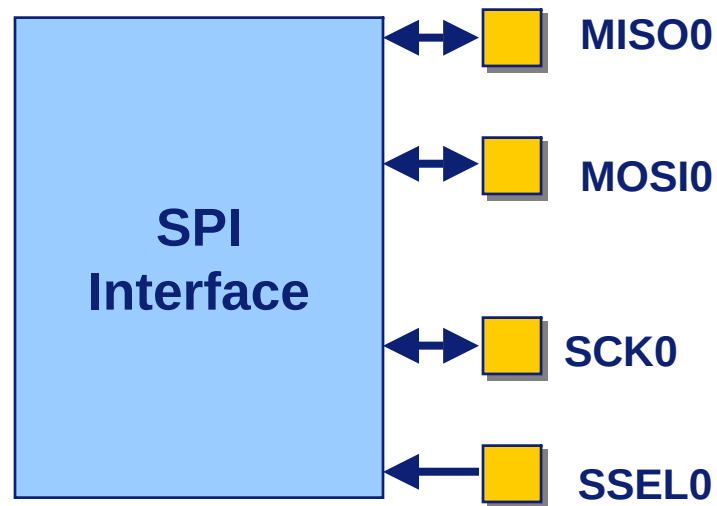
I²C Bus Interface

- Standard Fast-I²C compliant bus interface
 - 7-bit addressing
- Easy to configure as Master, Slave, or Master/Slave
- Programmable clocks allow versatile rate control
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)

I²C Bus Interface (cont.)

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization
 - allows devices with different bit rates to communicate via one serial bus
 - can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C bus interface can be used to connect I²C peripherals or for test and diagnostic purposes

SPI Interface

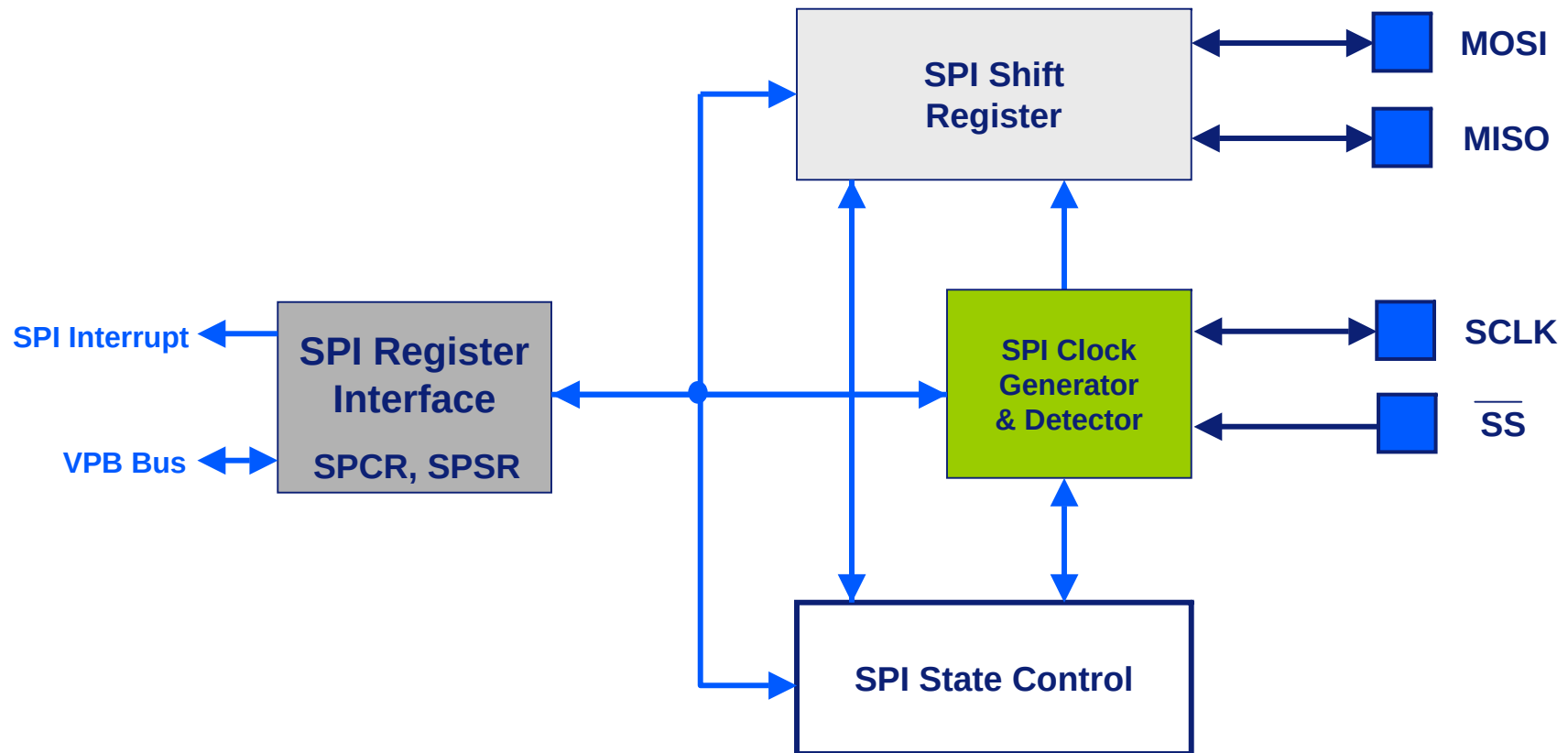


Maximum possible speed of the SPI
7.5 Mbits/sec

SPI Interface

- Compliant with Serial Peripheral Interface (SPI) specification
- Combined SPI master and slave function
- Maximum data bit rate of 1/8 of the peripheral clock rate
- Programmable settings for data transmit/receive operations
 - Clock polarity and clock phase
 - MSB / LSB first

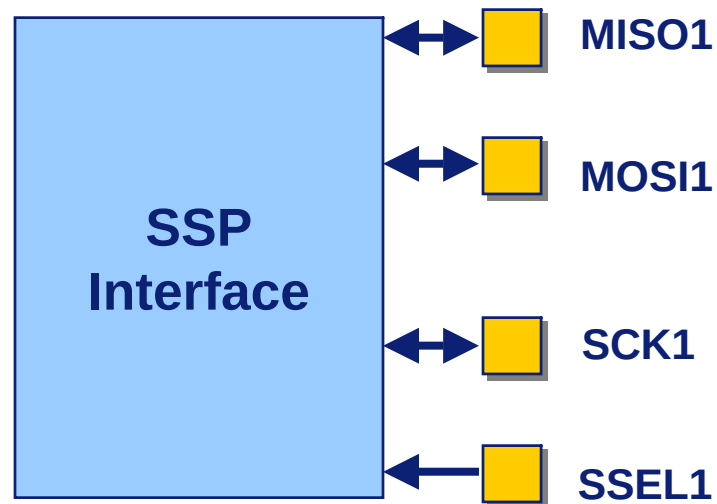
SPI Block Diagram



SPI Pin Descriptions

Pin Name	Type	Pin Description
SCK	Input/ Output	Serial Clock. The SPI is a clock signal used to synchronize the transfer of data across the SPI interface. The SPI is always driven by the master and received by the slave. The clock is programmable to be active high or active low. The SPI is only active during a data transfer. Any other time, it is either in its inactive state, or tri-stated.
SSEL	Input	Slave Select. The SPI slave select signal is an active low signal that indicates which slave is currently selected to participate in a data transfer. Each slave has its own unique slave select signal input. The SSEL must be low before data transactions begin and normally stays low for the duration of the transaction. If the SSEL signal goes high any time during a data transfer, the transfer is considered to be aborted. In this event, the slave returns to idle, and any data that was received is thrown away. There are no other indications of this exception. This signal is not directly driven by the master. It could be driven by a simple general purpose I/O under software control.
MISO	Input/ Output	Master In Slave Out. The MISO signal is a unidirectional signal used to transfer serial data from the slave to the master. When a device is a slave, serial data is output on this signal. When a device is a master, serial data is input on this signal. When a slave device is not selected, the slave drives the signal high impedance.
MOSI	Input/ Output	Master Out Slave In. The MOSI signal is a unidirectional signal used to transfer serial data from the master to the slave. When a device is a master, serial data is output on this signal. When a device is a slave, serial data is input on this signal.

Serial Synchronous Port (SSP) Interface



Maximum possible speed of the SSP
30 Mbits/sec

SSP Pin Descriptions

Freescale TI National Semiconductor

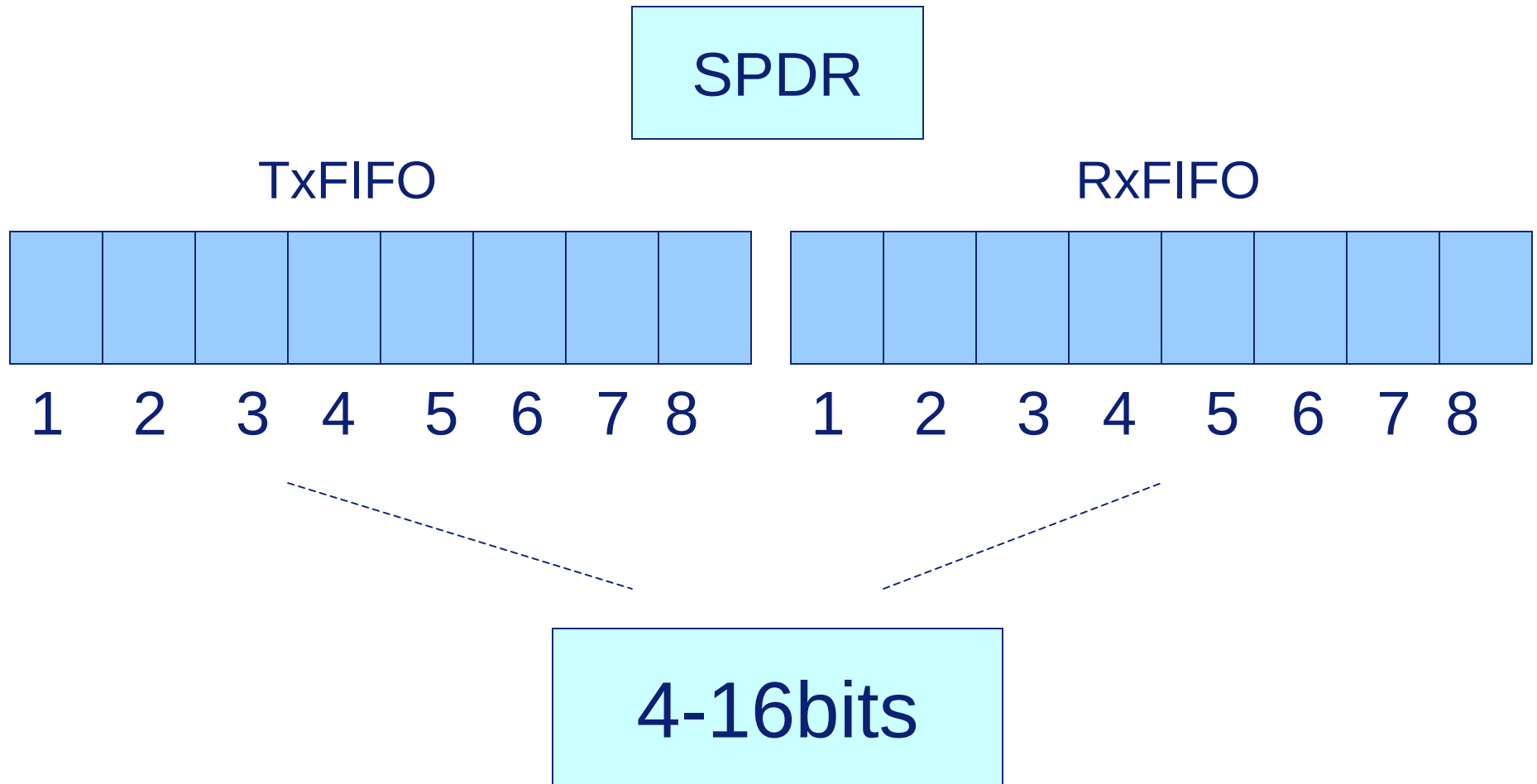
Pin Name	Type	Interface pin name/function			Pin Description
		SPI	SSI	Microwire	
SCK1	I/O	SCK	CLK	SK	Serial Clock. SCK/CLK/SK is a clock signal used to synchronize the transfer of data. It is driven by the master and received by the slave. When SPI interface is used the clock is programmable to be active high or active low, otherwise it is always active high. SCK1 only switches during a data transfer. Any other time, the SSP either holds it in its inactive state, or does not drive it (leaves it in high impedance state).
SSEL1	I/O	SSEL	FS	CS	Slave Select/Frame Sync/Chip Select. When the SSP is a bus master, it drives this signal from shortly before the start of serial data, to shortly after the end of serial data, to signify a data transfer as appropriate for the selected bus and mode. When the SSP is a bus slave, this signal qualifies the presence of data from the Master, according to the protocol in use. When there is just one bus master and one bus slave, the Frame Sync or Slave Select signal from the Master can be connected directly to the slave's corresponding input. When there is more than one slave on the bus, further qualification of their Frame Select/Slave Select inputs will typically be necessary to prevent more than one slave from responding to a transfer.
MISO1	I/O	MISO	DR(M) DX(S)	SI(M) SO(S)	Master In Slave Out. The MISO signal transfers serial data from the slave to the master. When the SSP is a slave, serial data is output on this signal. When the SSP is a master, it clocks in serial data from this signal. When the SSP is a slave and is not selected by SSEL, it does not drive this signal (leaves it in high impedance state).
MOSI1	I/O	MOSI	DX(M) DR(S)	SO(M) SI(S)	Master Out Slave In. The MOSI signal transfers serial data from the master to the slave. When the SSP is a master, it outputs serial data on this signal. When the SSP is a slave, it clocks in serial data from this signal.

Table 115: SSP Pin Descriptions

SSP Interface

- Compatible with Motorola SPI, 4-wire TI SSI and National Semiconductor Microwire bus
- Supports multiple slaves and master on the bus but at any point of time only one master and slave can communicate
- 8- Frame FIFO's for both Transmit and Receive
- Frame sizes can be from 4 bits to 16 bits

SSP Frames



SSP Interface

- Loop back mode supported
- Can generate interrupts when the buffer is half empty (for Tx) or half full (for Rx) along with Receive Overruns and time out

